## Remarks

Claims 7-9 are amended herein. Claims 1-2, 4-12, 14-17 and 19-20 remain pending in the Application.

## Rejection under 35 U.S.C. 112

In the Office Action, Claims 7-9 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The Claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 7-9 have been amended herein. Therefore, the rejection of Claims 7-9 is overcome.

## Rejection under 103(a)

### Claims 1-2, 4-5, 11-12, 14-17 and 19-20

In the Office Action, the Examiner rejected Claims 1-2, 4-5, 11-12, 14-17 and 19-20 under 35 USC 103(a) as being unpatentable over Tremblay et al. (hereinafter Tremblay) (6065108) in view of Burton et al (hereinafter Burton) (6738865). Applicant has reviewed the cited reference and respectfully submits that the present invention is not rendered obvious over Tremblay in view of Burton for the following rationale.

With respect to Claims 1, 11 and 16, Applicant respectfully states that Claims 1, 11 and 16 include the features of "blocks of code." Applicant understands the Examiner to state in the office action that Tremblay does not disclose the instruction cache is for storing a block of code, nor does Tremblay disclose tracking each time that said block of code is executed, nor does Tremblay disclose maintaining a storage area for storing counters associated with a block of code.

However, Applicant disagrees with the Examiners declaration that "if code is only a machine representation of some human-readable sequence of programming language, then programming instructions can be a block of such code, therefore, Tremblay has disclosed block of code in code cache.

Applicant respectfully submits that the present Invention discloses that a block of code being formed when the original source code is preprocessed to add a counter update instruction in each basic block code. The pre-processing step is static or "off-line", in that it takes place prior to the execution of the program. As a result, the programmer or tool must add counter code for every block that could ever execute." In addition, the program analysis with data caching system then performs the translation of the original source and inserts this translated program code into the code cache. A new program counter (NPC), which points to the beginning of the translated code, is returned for later execution during program analysis.

Applicant understands Tremblay to teach against the utilization of blocks of code instead of the original code. That is, Applicant understands Tremblay to teach against modifying the original instruction code to include the retrieved data and overwriting the original instruction code at the discrete location in the program memory with the modified instruction code. The modified instruction code is subsequently executed in place of the original instruction code. This is commonly referred to as self-modifying code. One disadvantage with self-modifying code is that once the original instruction code has been modified, the original instruction code is no longer available. The unavailability of the original instruction code can hamper subsequent program debugging. Another disadvantage is that the discrete location in the memory may not have sufficient capacity to store the modified instruction code (which includes the retrieved data). In certain prior art applications, the original instruction code is stored in a read only memory (ROM). In such applications, it is not possible to overwrite the original instruction code with a modified instruction code.

Therefore, Applicant understands Tremblay to teach away from the utilization of blocks of code. Thus, Applicant agrees with the Examiner's statement in the office action that Tremblay does not disclose the instruction cache is for storing a block of code, nor does Tremblay disclose tracking each time that said block of code is executed, nor does Tremblay disclose maintaining a storage area for storing counters associated with a block of code. But Applicant disagrees with the Examiner that any block of code references are rendered obvious in view of Tremblay and in fact are taught against by Tremblay.

Applicant does not understand Burton et al. to overcome the shortcomings of Holmberg. Specifically, Applicant does not understand Burton et al. to teach or render obvious the features of "a counter cache and a storage cache" both for storing counters. Accordingly, Applicant also respectfully submits that neither Tremblay alone or in combination with Burton et al. teaches or renders obvious the present claimed invention as recited in Claims 1, 11 and 16, and as such, Claims 1, 6, and 16 are in condition for allowance.

Applicant respectfully points out that Claims 2 and 4-5 depend from the allowable Independent Claim 1, Claims 12 and 14-15 depend from the allowable Independent Claim 11 and Claims 16-17 and 19-20 depend from the allowable Independent Claim 16 and recite further features of the present claimed invention. Therefore, Applicant respectfully states that Claims 2, 4-5, 11-12, 14-17 and 19-20 are allowable as pending from an allowable base Claim.

Claims 6-10

In the Office Action, the Examiner rejected Claims 6-10 under 35 USC 103(a) as being unpatentable over Holmberg (2001/0021959) in view of Burton. Applicant has reviewed the cited reference and respectfully submits that the present invention is not rendered obvious over Holmberg in view of Burton for the following rationale.

With respect to Claim 6, Applicant respectfully states that Claim 6 includes the features of "a counter cache and a storage cache" both for storing counters. Applicant understands the Examiner to state in the office action that Holmberg does not disclose maintaining a counter cache for storing a counter associated with a block of code, nor does Holmberg disclose maintaining a storage area for storing counters associated with a block of code.

Applicant understands Holmberg to teach against cache allocation based only on frequency of use. Applicant understands Holmberg to teach the utilization of additional features for cache allocation such as importance of the instruction. For example, Applicant understands Holmberg to teach that the processor can do measurements that do not count accesses from these program blocks or discard accesses made from programs running on lower priority levels. Therefore, Applicant understands Holmberg to teach away from the utilization of frequency for programs running on lower priority levels. Therefore, Holmberg neither teaches nor render obvious the features of the present invention.

Applicant does not understand Burton to overcome the shortcomings of Holmberg. Specifically, Applicant does not understand Burton to teach or render obvious the features of "a counter cache and a storage cache" both for storing counters. Moreover, Applicant does not understand Burton to teach cache allocation based on frequency of use. Accordingly, Applicant also respectfully submits that neither Holmberg alone or in combination with Burton teaches or renders obvious the present claimed invention as recited in Claim 6 and as such, Claim 6 is in condition for allowance.

Applicant respectfully points out that Claims 7-10 depend from the allowable Independent Claim 6 and recite further features of the present claimed invention. Therefore, Applicant respectfully states that Claims 7-10 are allowable as pending from an allowable base Claim.

## Conclusion

In light of the above amendments and remarks, Applicant respectfully requests allowance of Claims 1-2, 4-12, 14-17 and 19-20.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present application.

Respectfully submitted,
Wagner, Murabito & Hao LLP

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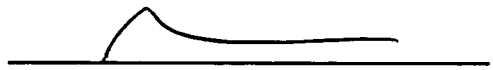

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